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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/715,295	11/17/2000	Tsunemasa Hayashi	10746/22	5885

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NEW YORK, NY 10004

EXAMINER

STEVENS, ROBERTA A

ART UNIT	PAPER NUMBER
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2665

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/715,295

Applicant(s)

HAYASHI ET AL.

Examiner

Roberta A Stevens

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 November 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 1 is/are withdrawn from consideration.
- 5) ☐ Claim(s) is/are allowed.
- 6) ☒ Claim(s) 1-6, 9, 11 and 13-15 is/are rejected.
- 7) ☐ Claim(s) 7,8,10,12,16 and 17 is/are objected to.
- 8) ☐ Claim(s) are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. .
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. <u> </u> |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3</u> | 6) <input type="checkbox"/> Other: <u> </u> |

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-6, 9, 11 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yonezawa (U.S. 5475825).

2. Regarding claim 1, Yonezawa teaches (abstract and figures 1-3 and 13) a data selection apparatus comprising: search units each of which includes table search circuits and a first circuit which performs a first selection process in which a table search circuit which outputs data is selected from table search circuits each of which succeeds in a search based on input data; and a second circuit which performs a second selection process in which each unit which output data is selected from search units, each of which includes a table search circuit which succeeds in a search wherein, when the first circuit receives a first signal which indicates that there is a table search circuit which succeeds in a search, the first circuit sends a second signal to the second circuit before performing the first selection process, the second signal indicating that there is at least one table search circuit which succeeds in a search; the second circuit performs the second selection process when the second circuit receives the second signal; and a search unit which is selected by the second selection process outputs data (columns 9-11).

3. Regarding claims 2 and 14, Yonezawa teaches (abstract and figures 1-3 and 13) each search unit has a third circuit outside of the first circuit, which send the first signal to the second

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circuit; and the first circuit performs the first selection process at the same time as when the third circuit sends the signal.

4. Regarding claims 3 and 11, Yonezawa teaches (abstract and figures 1-3 and 13) each table search circuit is a CAM.

5. Regarding claim 4, Yonezawa teaches (abstract and figures 1-3 and 13) each of the table search circuits includes a RAM and a MPU.

6. Regarding claim 5, Yonezawa teaches (figures 4, 7, 10 and 12) the first circuit includes a CAM output control circuit including small-scale logic circuits divided by flip flops in which time series pipeline processing is performed; and the second circuit also includes small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed.

7. Regarding claim 6, Yonezawa teaches (abstract and figures 1-3 and 13) a data selection apparatus comprising: search units comprises table search circuit and a data output control circuit, the table search circuit selecting data from a stored data table, which data includes an entry matching a search key which is a bit sequence of a part of input data, the data output control circuit performing a first selection process in which the highest priority output data is selected from outputs of the search units; data search success signal output means which sends a data search success signal to the data output control circuit from a hit circuit which is a table search circuit which succeeds in a search; and unit search success signal output means which sends a unit search success signal indicating that there is at least the hit circuit in the search unit to the unit output control device before the data output control device performs the first selection process; wherein, the data output control device starts the first selection process upon receiving the data search success signal and the unit output control device starts the second selection

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process upon receiving the unit search success signal; and a data output circuit in a search unit which is selected by the unit output control device selects output data of a table search circuit (columns 9-11).

8. Regarding claim 9, Yonezawa teaches (figures 4, 7, 10 and 12) the data output control circuit includes a CAM output control circuit including small-scale logic circuits divided by flip flops in which time series pipeline processing is performed; and the unit output control device also includes small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed.

9. Regarding claim 13, Yonezawa teaches (abstract and figures 1-3 and 13) a packet processing apparatus including a data selection apparatus, comprising: search units including table search circuits and a first circuit which performs a first selection process in which a table search circuit which outputs data is selected from table search circuits each of which succeeds in a search based on an input packet; and a second circuit which performs a second selection process in which each unit which output data is selected from search units, each of which includes a table search circuit which succeeds in a search wherein, when the first circuit receives a first signal which indicates that there is a table search circuit which succeeds in a search, the first circuit sends a second signal to the second circuit before performing the first selection process, the second signal indicating that there is at least one table search circuit which succeeds in a search; the second circuit performs the second selection process when the second circuit receives the second signal; and a search unit which is selected by the second selection process outputs data, the data being used as a destination address to which the input packet is transferred (columns 9-11).

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10. Regarding claim 15, Yonezawa teaches (abstract and figures 1-3 and 13) a packet processing apparatus including a data selection apparatus, comprising: search units comprises table search circuit and a data output control circuit, the table search circuit selecting data from a stored data table, which data includes an entry matching a search key which is a bit sequence of a part of input data, the data output control circuit performing a first selection process in which the highest priority output data is selected from outputs of the search units; data search success signal output means which sends a data search success signal to the data output control circuit from a hit circuit which is a table search circuit which succeeds in a search; and unit search success signal output means which sends a unit search success signal indicating that there is at least the hit circuit in the search unit to the unit output control device before the data output control device performs the first selection process; wherein, the data output control device starts the first selection process upon receiving the data search success signal and the unit output control device starts the second selection process upon receiving the unit search success signal; and a data output circuit in a search unit which is selected by the unit output control device selects output data of a table search circuit, the output data being used as a destination address to which the input packet is transferred (columns 9-11).

Allowable Subject Matter

11. Claims 7, 8, 10, 12, 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Srinivasan (U.S. 6460112 B1), Loschke (U.S. 5956336), Srinivasan (U.S. 6237061 B1) and Khanna (U.S. 6539455 B1) are cited to show the state of the art.

13. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Roberta Stevens whose telephone number is (703) 308-6607. The examiner can normally be reached on Monday through Friday from 9:00 am to 5:30 p.m.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor can be reached on (703) 308-6602.

15. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 305-3900.

16. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9306

For informal draft communications, please label "PROPOSED" or "DRAFT"

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,

Arlington, VA. Sixth Floor (Receptionist).

Roberta A. Stevens

Patent Examiner

03-21-04



STEVEN H. D. NGUYEN
PRIMARY EXAMINER